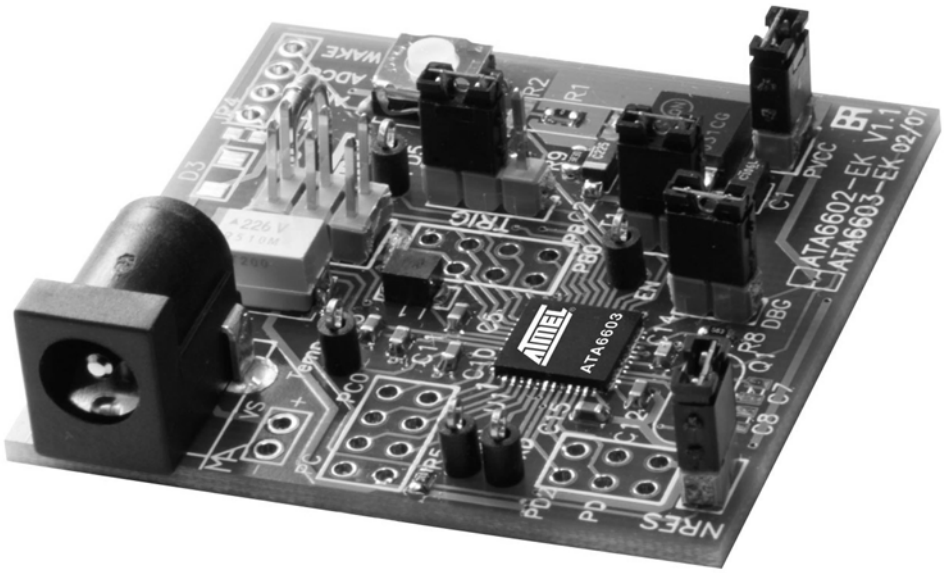
ATA6602/ATA6603 - EK
Development Board V1.1



Features

- All Necessary Components to Put the ATA6602/ATA6603 in Operation Are Included
- Placeholders for Some Optional Components for Extended Functions Included
- All Pins Easily Accessible
- Easily Adaptable Watchdog Times by Replacing a Single Resistor
- Possibility to Activate an External NPN-transistor for Boosting Up the Output Current of the Voltage Regulator (Jumper JP3)
- Possibility of Selecting between Master or Slave Operation (Mounting D3 and R4)
- Possibility to Mount an External Quartz to Handle Time-critical Applications (Not Necessary for LIN Communication)
- Push button Included for Creating a Local Wake-up after Having Entered the Sleep or Silent Mode
- Ground Coulter Clip for Connecting Probes Easily when Measuring with the Oscilloscope

ATA6602/ ATA6603 - EK Development Board V1.1

Application Note

4999C–AUTO–03/08

1. Introduction

The development board for the ATA6602/ATA6603 IC is designed to give designers a quick start with the ATA6602 and ATA6603 ICs and to enable prototyping and testing new LIN designs.

The ATA6602 and ATA6603 form a single-package dual-chip circuit family for LIN-bus slave and master node applications. They support highly integrated solutions for in-vehicle LIN networks. The LIN-system-basis-chip (LIN-SBC) consists of a voltage regulator, a window watchdog, and a fully integrated LIN transceiver, which is in accordance with the LIN specification 2.0. The second chip is a microcontroller from Atmel®'s series of AVR® 8-bit microcontrollers with advanced RISC architecture (Atmega88 in ATA6602 and the Atmega168 in ATA6603).

The ATA6602 and ATA6603 provide the following features:

- 8/16 Kbytes of in-system programmable flash with read-while-write capabilities
- 512 bytes EEPROM
- 1 Kbyte SRAM
- 23 general purpose I/O lines
- 32 general purpose working registers
- 3 flexible timer/counters with compare modes
- Internal and external interrupts
- Serial programmable USART
- Byte-oriented 2-wire serial interface
- SPI serial port
- 8-channel 10-bit ADC
- Five software-selectable power-saving modes:
  - Idle Mode stops the CPU while allowing the SRAM, timer/counters, USART, 2-wire serial interface, SPI port, and interrupt system to continue functioning.
  - Power-down Mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.
  - Power-save Mode: the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping.
  - ADC Noise Reduction Mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions.
  - Standby Mode: the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The combination of features included in ATA6602 and ATA6603 make it possible to develop simple, but powerful and cheap slave nodes in LIN bus systems.

The ICs are designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud. Sleep Mode and Silent Mode included in the LIN-SBC guarantee a very low current consumption.

The ATA6602 and the ATA6603 are completely pin and functional compatible. They differ only in the size of the flash memory of the integrated microcontroller. Some minor modifications in the source code when switching between ATA6602 and ATA6603 during the development phase may be required. For more information concerning this topic, refer to the application note AVR095: “Migrating between ATmega48, ATmega88 and ATmega168” available at http://www.atmel.com.

As there is a standard AVR microcontroller with all pins available included in the ATA6602 and ATA6603, the standard toolchain consisting of the AVR Studio®, front-end assembler and simulator, and in-circuit-emulator can be used for developing and debugging new applications. ActiveX® components are also available that can be used to create a simple PC program for emulation of the LIN master node. Using the software components and the development board, it is very easy and inexpensive to create and test a LIN network.

This document has been developed to provide the user with start-up information about the ATA6602 and ATA6603’s development board. For more detailed information about the use of the devices themselves, refer to the corresponding datasheet.

2. Quick Start

The development board for the ATA6602 and ATA6603 is shipped with the default jumper settings and all accessories required for immediate use.

The IC mounted on the board is pre-programmed with a firmware in order to test and to understand the basic functions directly on the board. After correctly connecting an external 12V DC power supply between the terminals “+” and “-”, the LIN-SBC is in Pre-normal Mode. A regulated 5V DC voltage, provided by the internal voltage regulator supplying the internal microcontroller, can be measured at the PVCC jumper. After the power is supplied to the microcontroller, the microcontroller switches the LIN-SBC to Normal Mode by setting the EN pin to high (test pin PORTD.7 - EN), and starts to trigger the integrated window watchdog. The system is now ready for data transmission via the LIN bus. Signals fed in at the TXD pin are visible on the LIN bus, and signals fed in on the LIN bus are visible at the RXD pin. In Normal Mode, the current consumption is approximately 8 mA to 9 mA and the following voltages can be measured against ground at the various pins.

Table 2-1. Overview of Pin Status at Start-up of the Development Board

	VCC	TEMP	EN	TXD	RXD	NRES	TRIG (Middle Pin)	LIN	Transceiver
Normal Mode	5V	2.0V to 2.35V	5V	5V	5V	5V	0V to 5V with 70 Hz	recessive	On

The board’s pre-programmed firmware provides the window watchdog with a valid trigger signal so that the NRES pin is not forced to ground and the microcontroller does not receive any resets.

For testing purposes and to understanding the system, it can be helpful to see the behavior when the watchdog is not triggered correctly. This can be achieved in three different ways without changing the firmware of the IC:

- Remove TRIG jumper
  No trigger signal reaches the watchdog and the watchdog generates a reset directly after the lead time t_d (51kΩ) = 49 ms has expired.
- Remove RWD jumper
  The trigger signal for watchdog times according to a 51 kΩ resistor are not valid anymore, because the resistor for adjusting the watchdog timing is disabled resulting in different watchdog times. This will result in generating a reset, because the trigger pulses not occurring in the open window of the window watchdog
- Re-program the Fuse bit
  Changing the fuse bit CKDIV8 to un-programmed, changes the microcontroller’s internal clock from 1 MHz to 8 MHz. Because of this the trigger signals generated from the microcontroller does not meet the open window from the window watchdog and a reset is generated.

3. Hardware Description

3.1 Pin Description

In the following sections the external elements required for some of the pins will be shown and described. For further information about this topic, refer to the relevant datasheet.

3.1.1 Power Supply (VB and GND)

In order to get the development board running, an external 5.7V to 18V DC power supply has to be connected to the power connector (positive center connector) or to the terminals “+” and “-” directly underneath the power connector. The input circuit is protected against inverse-polarity with the protection diode D1. This causes a difference of approximately 0.7V between the supplied voltage V_{Bat} and the voltage at the VS pin.

3.1.2 Voltage Regulator (PVCC and VCC)

The internal 5V voltage regulator is capable of driving loads with up to 50 mA current consumption. Therefore, the ATA6602 and ATA6603 are able to supply the internal microcontroller, some external sensors, and/or other ICs required for the LIN node. The voltage regulator is protected against overloads by means of current limitation and overtemperature shutdown. To boost the maximum load current, an external NPN transistor may be used. Its base is connected to the VCC pin and its emitter is connected to PVCC. To enable this feature, the jumper PVCC, which connects the two pins PVCC and VCC by default, has to be removed.

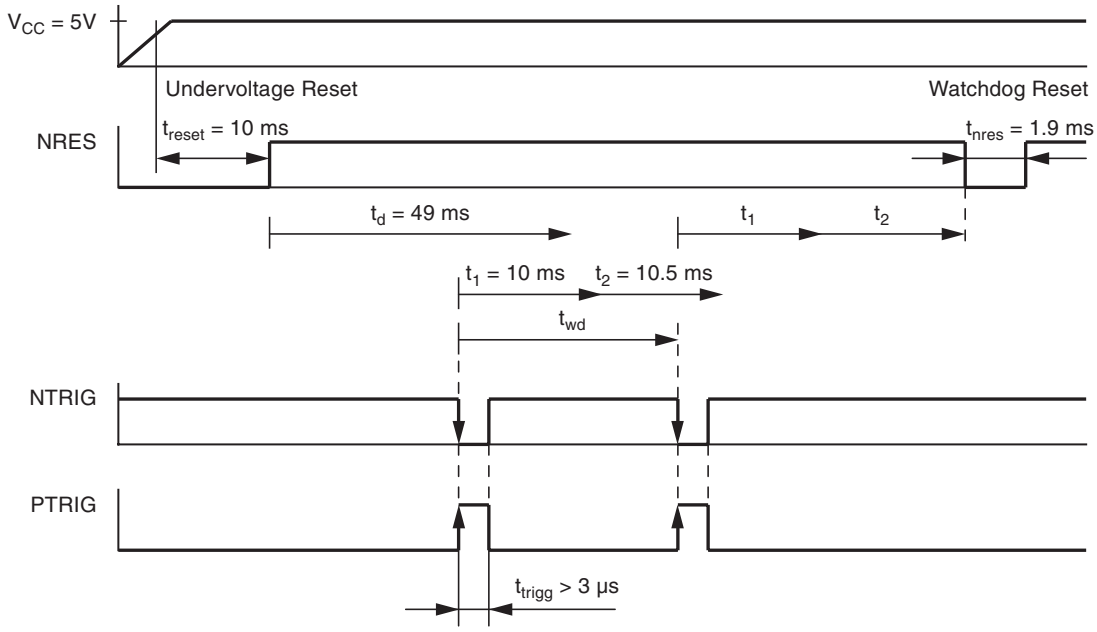
As for the most applications 50mA will be sufficient the jumper PVCC can remain set.

3.1.3 The Window Watchdog (PTRIG, NTRIG, WD_OSC and NRES)

The watchdog anticipates a trigger signal from the microcontroller at the NTRIG input (negative edge) or at the PTRIG input (positive edge) within a defined time window. If no correct trigger signal is received during the open window, a reset signal (active low) will be generated at the NRES output. During Silent Mode or Sleep Mode the watchdog is switched off to reduce current consumption.

The timing basis of the watchdog is provided by the internal oscillator, whose time period t_{OSC} is adjustable via the external resistor R8 at the WD_OSC pin. All watchdog-specific timings (t_1, t_2, t_d, ...) are based on the value of this resistor. By default there is a resistor with a value of 51 kΩ mounted on the development board, which results in the following timing sequence for the integrated watchdog.

Figure 3-1. Watchdog Timing Sequence with R8 = 51 kΩ



The microcontroller pin PD6 is used by default to trigger the watchdog. In order to lead the signals generated from pin PD6 to the watchdog trigger input NTRIG or PTRIG, the jumper TRIG has to be set accordingly. If it is not possible to use the pin PD6 to trigger the watchdog as it is being used for another function, remove the TRIG jumper completely and connect either the NTRIG pin or the PTRIG pin directly to another microcontroller pin using a 1-wire cable.

The unused trigger input can be left open on the development board, as trigger inputs are equipped with an internal pull-up (NTRIG) or pull-down (PTRIG) resistor. For normal use of ATA6602 and ATA6603, it is recommended that trigger input pin not used to trigger the watchdog, is tied directly either to VCC for NTRIG or to ground for PTRIG.

Replacing the resistor R8 results in a frequency change of the internal oscillator. This in turn results in different watchdog timing. The following formula demonstrates how the frequency of the internal oscillator depends on the value of the resistor R8. Refer also to the ATA6602/ATA6603 datasheet for further information:

$$t_{OSC}[R_{WD\_OSC}] = -0.00007 \times (R_{WD\_OSC})^2 + 0.25 \times R_{WD\_OSC} + 0.067$$

t_{OSC} in µs

R_{WD_OSC} in kΩ

With the values given in the datasheet, you can calculate all relevant watchdog times (for example the open window and the closed window) using t_{OSC}.

In general, both ATA6602 and ATA6603 are shipped with an oscillator start-up time of 65 ms. Therefore, in most cases it is necessary to reduce this start-up time to 0ms or 4.1 ms via the fuse settings in order to meet the first open window. The IC mounted on the board is delivered with a start-up time of 0 ms.

3.1.4 LIN Interface (LIN, TXD and RXD)

The LIN Transceiver is only active when the LIN-SBC is in the normal mode. In all other modes the transceiver is switched off and no signals from the microcontroller will be transmitted on the bus and no signals from the bus will be given to the microcontroller.

As the two pins TXD and RXD on the LIN-SBC are controlled by the microcontroller's UART, they are directly connected to the corresponding TXD and RXD pins on the microcontroller. For monitoring the signals at these pins, test points have been provided on the development board.

3.1.4.1 LIN Pin

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor in compliance with LIN spec 2.0 are implemented. LIN receiver thresholds are compatible with the LIN protocol specification.

At the LIN pin there is a 220 pF capacitor to ground on the board. Additionally, when using the development board for a LIN master application, it is possible to mount the two necessary extra components diode D3 (e.g., LL4148) in series with resistor R4 (1 kΩ) on the board at their designated placeholders.

3.1.4.2 TXD Input/Output Pin (LIN-SBC)

The signals given to the TXD input pin control the state of the LIN output. The TXD input pin must be pulled to ground in order to have the LIN bus low. If TXD is high, the LIN output transistor is turned off and the bus is in recessive state, pulled up by the internal/external resistor. If TXD is low, the LIN output transistor is turned on and the bus is in dominant state. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 6 ms, the LIN-SBC switches the TXD state internally to high and the LIN bus driver is switched to the recessive state.

This feature is used to avoid that either a single faulty slave node or a short to ground at the TXD pin can paralyze the communication on the complete LIN bus to which the faulty slave node is connected. Due to this behavior, the internal state of the TXD pin can differ from the signal level visible at the pin itself. However, for the LIN-SBC itself, the internal state of the TXD pin is more important and the SBC reacts to this state (e.g., switching to Silent Mode instead of Sleep Mode due to having pulled TXD to low too early).

3.1.4.3 TXD Input/Output Pin (Microcontroller)

The TXD-pin from the microcontroller, belonging to the hardware UART, is hard-wired to the TXD input pin from the LIN-SBC.

As the LIN-SBC indicates the wake-up source (local wake-up or remote wake-up) with the help of the TXD pin it is recommended that the TXD pin from the microcontroller will be reconfigured as an input when entering silent mode or sleep mode. As long as pin EN is still low after a wake-up the LIN-SBC signals the wake-up source on pin TXD.

3.1.4.4 RXD Output Pin (LIN-SBC)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD; LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up structure with typically 5 kΩ to VCC.

This output is short-circuit protected.

3.1.5 Temp Pin (LIN-SBC)

Besides the internal temperature monitoring of the voltage regulator, an additional integrated temperature sensor measures the junction temperature and provides a linearized voltage at the TEMP pin. On the development board, the TEMP pin is connected to the microcontroller's Analog-Digital-Converter input pin ADC7.

For measuring the internal junction temperature of the LIN-SBC, the user can choose between providing an external reference voltage or using the regulated 5V voltage from the internal voltage regulator as reference voltage.

A test pin is provided for easy access to the TEMP pin for comparative measurements.

If the TEMP pin is not used in the application, it should be connected directly to ground.

3.1.6 ADC7 (Microcontroller)

As the ADC7 can only be used for converting analog signals to digital values, this pin has been chosen for measuring the junction temperature of the LIN-SBC: the hottest temperature within the whole IC. This enables the application to detect overload conditions. Further actions in order to prevent the IC from damage can be implemented.

This analog input is equipped with a ceramic capacitor in order to stabilize the output voltage from the TEMP pin.

3.1.7 ADC6 (Microcontroller)

As the ADC6 can only be used for converting analog signals to digital values, and there is no analog output from the ATA6602 and ATA6603 to measure apart from the TEMP pin, the ADC6 has been led off the board in order to be externally connected if required. The analog input is equipped with a ceramic capacitor in order to stabilize the analog voltage connected to this pin.

3.1.8 PD5 (Microcontroller)

This pin is intended for generating trigger pulses for measurements using an oscilloscope. When monitoring some signals it might be helpful not to trigger on the signal itself, but instead on a selectable trigger-point in time. For this purpose, pin PD5 is equipped with a test pin to connect probes.

3.1.9 WAKE (LIN-SBC)

The high-voltage input pin, WAKE, can be used to generate a local wake-up from Sleep Mode or Silent Mode. A push button is provided at this pin on the development board. If a local wake-up is not required in the application, the WAKE pin should be connected to VS. If this connection is made, resistors R6 and R7 need to be replaced by 0Ω resistors.

3.1.10 MODE Pin (LIN-SBC) and Debug Mode

During the early development phase it can be helpful to deactivate the watchdog so that no resets disturb the normal application program. It is strongly recommended to use this so-called Debug Mode only during the development phase as the watchdog is an important safety feature for the most applications used in automotive environment.

On the development board the MODE pin is pulled to ground via the 10 kΩ resistor R3. Therefore, the watchdog is active during LIN-SBC's Normal Mode or Pre-normal Mode. By setting the DBG jumper, the MODE pin is tied to 5V, and the watchdog is disabled. If the watchdog is disabled, the other reset sources (undervoltage reset and after power-up) remain active. In order to avoid reset of the microcontroller during debugging deactivate the watchdog and remove the jumper NRES.

Please note, if the jumper NRES has been removed and an undervoltage occurs the LIN-SBC switches to Pre-normal Mode irrespective of whether the microcontroller has been reset or not. In this case, the LIN transceiver is deactivated as long as the reset line is low due to the undervoltage.

3.1.11 NRES Output Pin (LIN-SBC) and PC6/NRES Input Pin (Microcontroller)

In addition to the normal behavior of the NRES pin as the executing pin of watchdog failures (and of undervoltage detection) already described in Section 3.1.3 "The Window Watchdog (PTRIG, NTRIG, WD_OSC and NRES)" on page 5, there are some special considerations that should be taken into account when using this pin together with a microcontroller like the ATA6602 or ATA6603.

The NRES output pin of the LIN-SBC is connected to the NRES input pin (PC6) of the microcontroller via the jumper "NRES". For normal operation, this jumper has to be set so that a reset signal generated from the LIN-SBC will reset the microcontroller. However, for the following three cases it is necessary to remove this jumper:

- Testing in general (for an example please refer to Section 3.1.10 "MODE Pin (LIN-SBC) and Debug Mode" on page 9)
- Debugging via Debugwire (for further information please refer to Section 4.2 "Debugging the ATA6602/ATA6603" on page 14)
- Programming the microcontroller (for further information please refer to Section 4.1 "Programming the ATA6602/ATA6603" on page 14)

If the jumper has been removed, the 10 kΩ pull-up resistor R5 keeps the reset line high, so that the reset input pin has a defined level and the microcontroller will not be reset by interferences.

3.1.12 PB6 and PB7 (Microcontroller)

The microcontroller runs on an internal RC-oscillator with a default frequency of 1 MHz. As the accuracy of the internal clock is sufficient for LIN communication, in most cases there is no need for higher accuracy. However, for some applications a more accurate clock is required and therefore an external crystal oscillator can be mounted on the development board at the designated placeholder Q1 together with the required capacitors C7 and C8 (please refer also to Section 3.4.2 "Running the Microcontroller on External Clock" on page 13). Please note, that when activating the external clock, the fuse bit setting has to be changed. For more information about how to change the fuse bits and information on using an external clock, refer to the datasheet of the ATA6602/ATA6603 and to the AVR Studio documentation.

3.1.13 Other pins

All remaining pins not described in this section do not have any special external circuitry and/ or they are used as described in details in the datasheet.

3.1.14 Summary of the Hard-wired Pins on the ATA6602/ATA6603 - EK

As already described in detail in the previous sections, there are some pins tied together on the development board in hand. Table 3-1 gives a summary of these pins.

Table 3-1. Summary of the Hard-wired Pins on the ATA6602/ATA6603 - EK

Microcontroller Pin ...	... Is Connected to LIN-SBC Pin ...
PC6/NRES	NRES
PD6	PTRIG/NTRIG
PD0	**RXD**
PD1	**TXD**
PD7	**EN**
ADC7	**TEMP**

The four connections marked in **bold** are equipped with a test point in order to gain access to them for measurement purposes. The other two connections are generated via a jumper and therefore are easy to access.

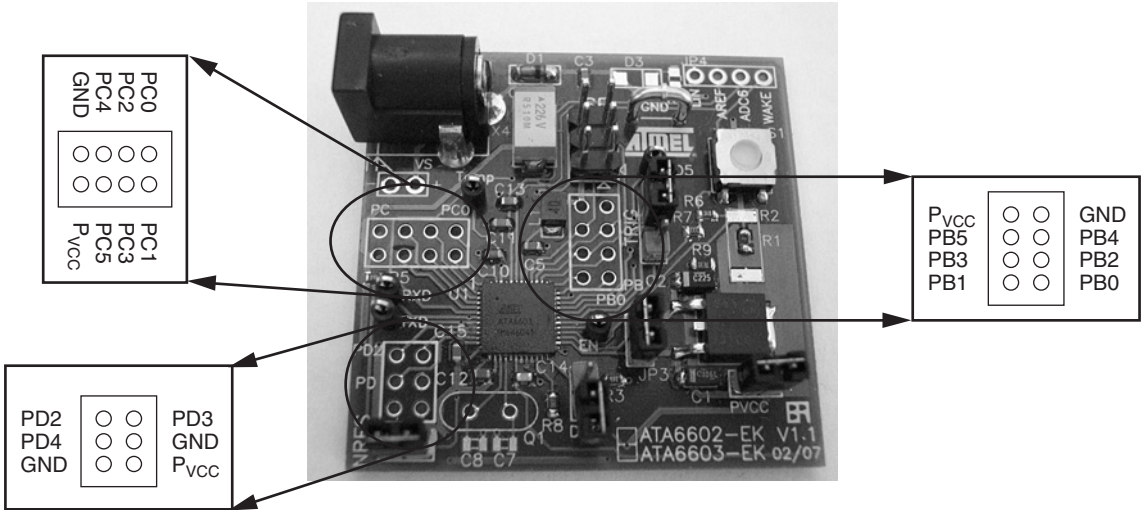
Pin PD5 is also equipped with a test point.

3.2 Port Connectors

The ATA6602/ATA6603-EK has three port connectors for the microcontroller ports PortB, PortC, and PortD. All non-reserved I/O-pins available from the microcontroller are routed to the corresponding connectors to give the user easy access to them. All three connectors provide, besides the port pins, a voltage supply pin (5V from the internal voltage regulator) and at least one ground pin in order to easily connect application-specific add-ons.

The pinouts of the three connectors are shown in Figure 3-2.

Figure 3-2. Pinout of the Port Connectors



3.3 Jumper Description

In order to be more flexible and to meet as many requirements as possible, jumpers are provided on the development board. With the help of these jumpers, users have the opportunity to engage with the system itself in order to test some features and/or to adapt the system to their requirements. In the following sections all jumpers on the development board are briefly described. For additional information, check the previous sections.

3.3.1 Jumper NRES

By default, this jumper is set to generate a connection between the NRES output of the LIN-SBC and the reset input of the microcontroller. This results in a resetting of the microcontroller in the event of watchdog failures or undervoltage at the voltage regulator output. As already described earlier in this document, there are some cases in which it is helpful to remove this jumper (e.g., testing purposes, debugging, and programming of the microcontroller).

However, for normal operation of the LIN node, this jumper should be set.

3.3.2 Jumper TRIG

By default, this jumper is set to generate a connection between the watchdog trigger signal output pin PD6 from the microcontroller and the watchdog trigger signal input pin NTRIG from the LIN-SBC. This jumper can be set to trigger the watchdog via PTRIG. If pin PD6 is used for an alternative functions in the application, the TRIG jumper can be completely removed giving access to the PD6 pin. In this case, the watchdog has to be triggered by another I/O-pin from the microcontroller, and the connection to one of the trigger inputs has to be made via an extra 1-wire cable.

3.3.3 Jumper DBG

By default, this jumper is removed to apply a low-level at the MODE pin of the LIN-SBC via the pull-down resistor R3. In this case, the LIN-SBC's watchdog is active and expects trigger pulses from the microcontroller.

For debugging the application it is often useful to deactivate the watchdog in order to get no resets while staying at a break point for example. In this case, the DBG jumper has to be set which applies a high level at the MODE pin. From now on the watchdog is deactivated. More information about the Debug Mode can be found in Section 3.1.10 "MODE Pin (LIN-SBC) and Debug Mode" on page 9.

3.3.4 Jumper PVCC

By default, this jumper is set to generate a connection between the 5V output voltage of the LIN-SBC and the voltage supply pins of the microcontroller. For example, in order to determine the overall current consumption of the devices connected to the internal voltage regulator, the user can remove the jumper PVCC and interpose an ampere meter between the two now separated pins of the jumper PVCC.

3.3.5 Jumper JP3

By default, this jumper is set so that the internal 5V voltage regulator is active with a current ability of 50 mA; however, most LIN nodes require much less. For LIN nodes requiring more current, the current ability can be boosted with the help of a couple of additional external components. Refer to Section 6. on page 16 for a detailed description of how to boost the current ability of the voltage regulator.

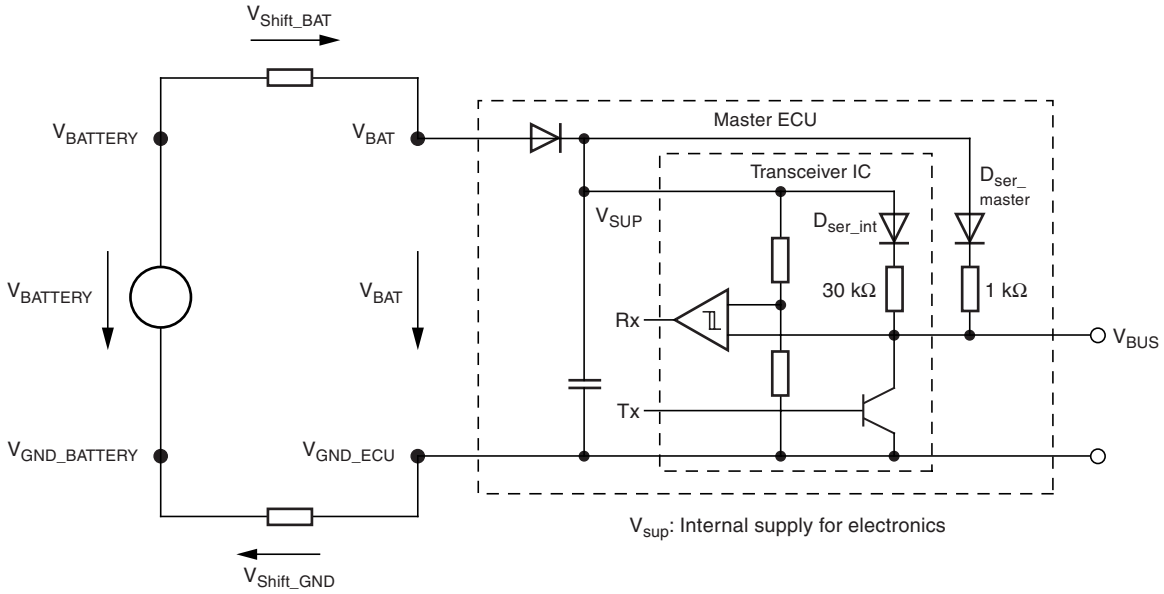
3.4 Optional components

The development board for the ATA6602/ATA6603 provides some placeholders for mounting additional, optional components. Some already mounted components can be replaced in order to adapt the LIN node to the users specific requirements. In the following sections these placeholders and components will be shown and described.

3.4.1 Configuring the ATA6602/ATA6603-EK as a Master or a Slave Node

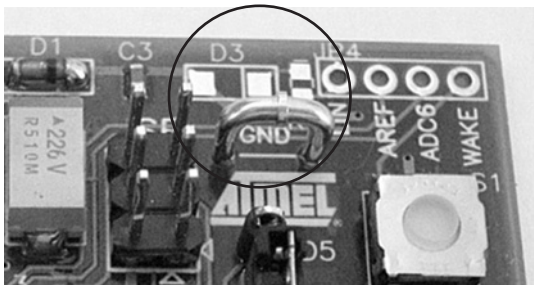
The LIN2.0 specification, as well as the LIN2.1 specification, stipulates that the master node in a LIN network has to be built up in the way depicted below.

Figure 3-3. External Circuitry for a LIN Master Node



The difference between a master node and a slave node is the additional diode D_{ser_master} together with a serial 1 kΩ resistor between V_{sup} and the LIN line. The placeholders for these two components D3 and R4 on the ATA6602/ATA6603 - EK are shown in Figure 3-4.

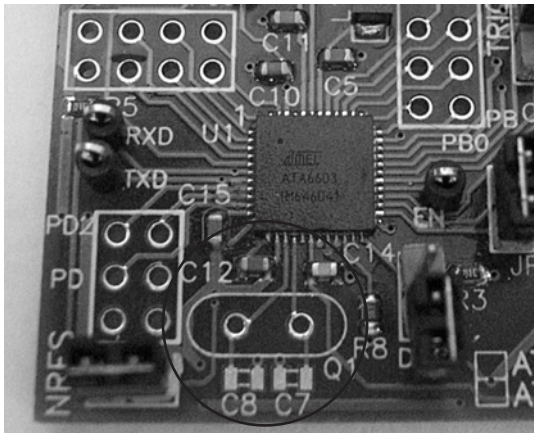
Figure 3-4. Placeholders for Diode and Resistor Necessary for LIN Master Applications



3.4.2 Running the Microcontroller on External Clock

For cases in which the accuracy of the internal RC-oscillator is not sufficient to meet the application specific requirements, there is the opportunity to mount an external crystal oscillator plus the two capacitors on the ATA6602/ATA6603 - EK. The location of these placeholders is shown in Figure 3-5.

Figure 3-5. Placeholder for External Crystal Oscillator Plus the Corresponding Capacitors

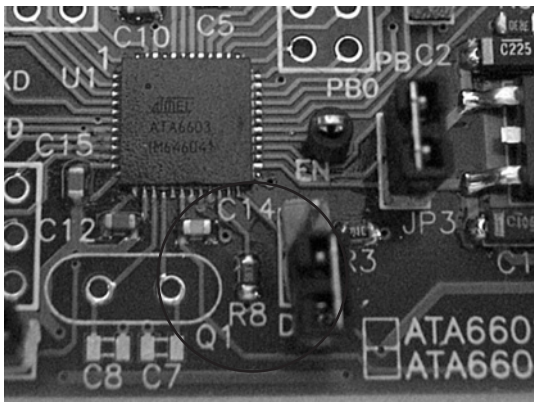


For the values of the two capacitors, check the datasheet of the desired oscillator.

3.4.3 Changing the Watchdog Timings

By default on the ATA6602/ATA6603 - EK, the watchdog timing is generated with the help of a 51 kΩ resistor (R8) connected between pin WD_OSC and ground. In order to change these timings, the resistor R8 has to be replaced. Its location is shown in Figure 3-6.

Figure 3-6. Location of Resistor R8



A description of how the resistor R8 influences the watchdog timing can be found in Section 3.1.3 “The Window Watchdog (PTRIG, NTRIG, WD_OSC and NRES)” on page 5 and in the ATA6602/ATA6603 datasheet.

4. Programming and Debugging the ATA6602/ATA6603

The easiest way to program and to debug the ATA6602/ATA6603 is to use the AVR Studio environment together with the STK500 or the JTAG-ICE MkII from Atmel. AVR Studio is an Integrated Development Environment (IDE) for writing and debugging AVR applications in Windows® 9x/Me/NT/2000/XP environments. AVR Studio provides a project management tool, source file editor, chip simulator, and In-circuit emulator interface for the powerful AVR 8-bit RISC family of microcontrollers.

4.1 Programming the ATA6602/ATA6603

Connect the selected hardware (STK500 or JTAG-ICE MkII) to the ISP header of the ATA6602/ATA6603 - EK via the 6-wire cable. Pin “1” is marked with two little triangles on the board. Before the programming session starts, remove the jumper NRES, as the programming tool needs exclusive access to the reset line during programming.

In the AVR Studio, the two devices ATA6602 and ATA6603 are not listed in the supported devices list, as they contain the standard devices Atmega88 and Atmega168 respectively. So to program the ATA6602, select the Atmega88 and to program the ATA6603, select the ATmega168.

For further information about using the STK500, the JTAG-ICE MkII or the AVR Studio, refer to the relevant documentation, which is available on the web.

4.2 Debugging the ATA6602/ATA6603

Combined with AVR Studio, the JTAGICE MkII can perform On-Chip Debugging on all AVR 8-bit RISC microcontrollers with JTAG Interface or debugWIRE interface. The ATA6602 and ATA6603 come with a debugWIRE interface so only a minimum of 3 wires is required for communication between JTAGICE MkII and the board. These Signals are RESET, VCC and GND.

The debugWIRE On-chip debug system uses a one-wire bi-directional interface to control the program flow, execute AVR instructions in the CPU, and to program the different non-volatile memories. To debug via debugWIRE, the reset line is used, and as the JTAG ICE MkII needs excusively access to this line, the jumper NRES has to be removed. The mounted pull-up resistor R5 does not disturb the debug session.

For more detailed information about debugging via the debugWIRE interface, refer to the relevant documentation, which is available on the web.

5. Tools

As already described briefly in the previous section, AVR Studio, in combination with the STK500 and JTAG ICE MkII, is a powerful tool for programming and debugging the AVR microcontroller family in general.

Furthermore, Atmel provides cost-effective software support for the development of a LIN network. These can easily be used together with the development board.

The first is a LIN2.0 ANSI C software library for the AVR microcontroller family in general. With the help of this, the protocol handling of LIN slave nodes can be programmed.

ActiveX-components also provided by Atmel, can be used to create a simple PC-program for emulating the LIN master node.

Using these software components, it is very easy to build up and to test a LIN network without much (financial) effort. The software tools will be available soon at http://www.atmel.com/products/Auto (go to tools).

Many OEMs demand that their suppliers use certified LIN protocol stacks from third party. To meet this requirement there is a LIN 2.0 protocol stack available for the ATA6602 (Atmega88) as well as for the ATA6603 (Atmega168) from Mentor Graphics. This LIN stack supports the developing of slave and master nodes. For more information concerning this tool please contact Mentor Graphics directly and/or check the following website:

http://www.mentor.com/products/vnd/in-vehicle_software/lin_target_package/index.cfm

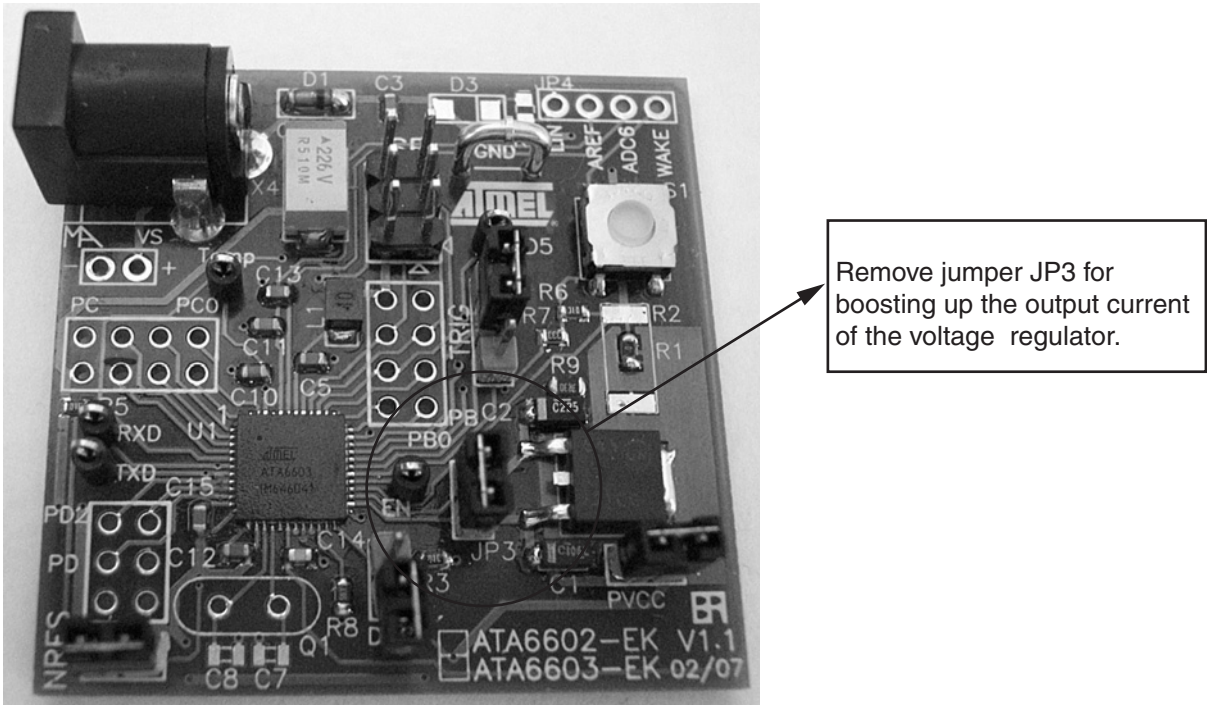
6. Boosting Up the Voltage Regulator

For some applications there is a requirement for a higher current than the internal voltage regulator can deliver (50 mA). In order to meet this requirement, it is possible to boost up the maximum current by using an external NPN transistor. A transistor, MJD31C in a D-PAK package, is already mounted on the development board, and in addition to the transistor there are two more components placed on the development board, the resistor R9 (3.3Ω) and the electrolytic capacitor C2 (2.2 µF). In addition, the jumper JP3 has to be removed when using the external transistor.

Note that the output voltage is no longer short-circuit protected when boosting up the output current with an external NPN transistor.

The limiting parameter for the output current is the maximum power dissipation of the external NPN transistor. In the version at this stage, the thermal resistance of the MJD31C soldered on the minimum pad size is 80 K/W. This means that the possible maximum output current in the case of V_S = 12V is approximately 230 mA at room temperature. It is not recommended to exceed this limit, as the transistor could be damaged as a result of overtemperature. If a higher output current is required, additional cooling of the external transistor has to be ensured (refer also to the diagrams in the appendix B).

Figure 6-1. Boosting Up the Voltage Regulator

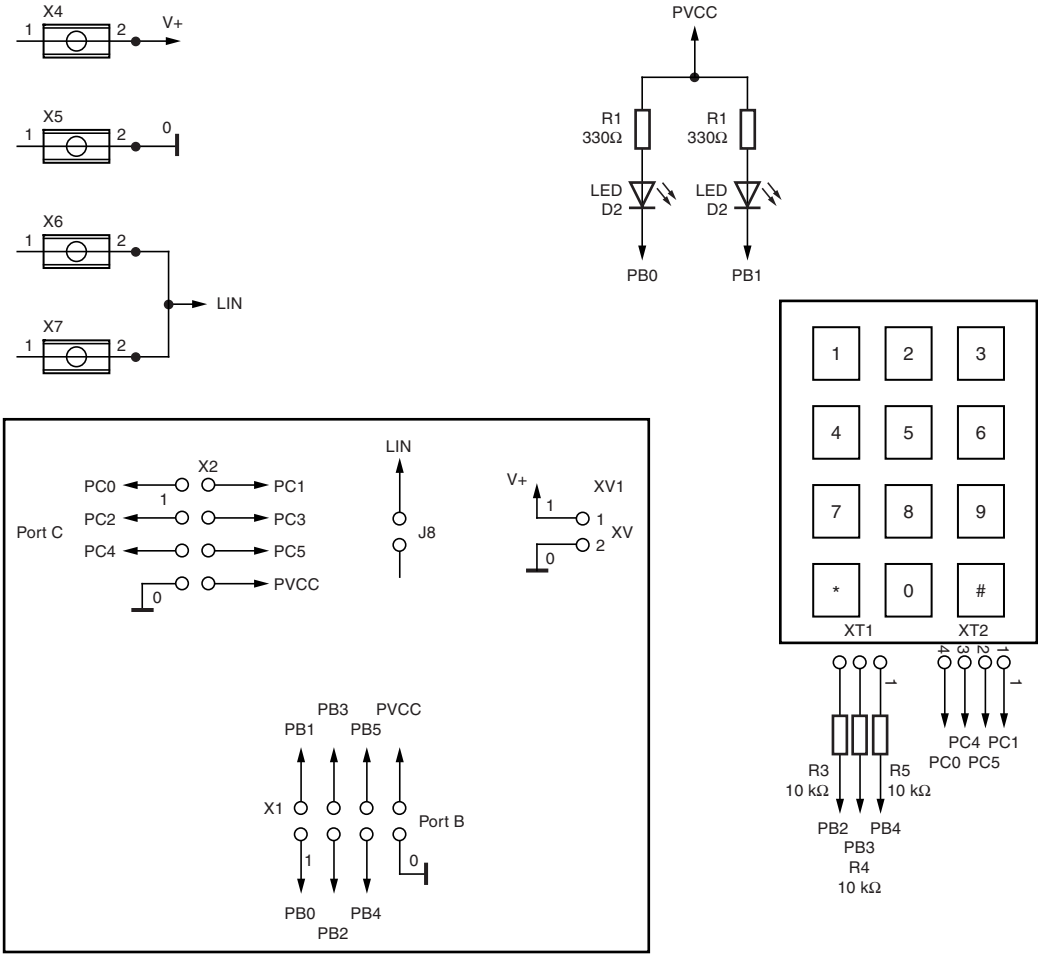


7. The Development Board in a Simple Application

Just to show how easy it is to develop a LIN based application with the development board for the ATA6602/ATA6603, here is a short example for a complete LIN slave node consisting of the ATA6602/ATA6603 - EK, a key matrix whose inputs will be transmitted via the LIN bus.

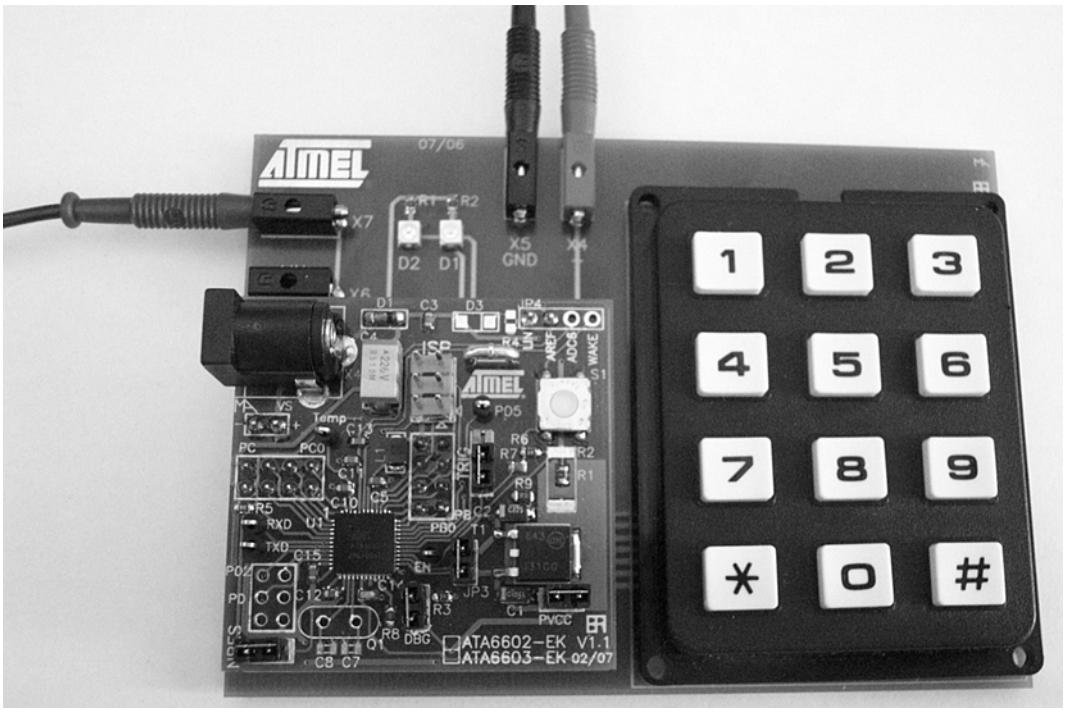
In the schematic of this slave node it is clear that there are almost no external components needed to fulfill the requirements of this application apart from the ATA6602/ATA6603 development board.

Figure 7-1. A Simple Application Using the Development Board for the ATA6602/ATA6603 (Schematic)



Two LEDs, five current limiting resistors, the power supply jack and the LIN jack are the only external components used for this application. From the development board there are only the required pins and connectors shown in the schematic above. In this application the board is plugged on another board containing the key matrix and the additional components. Figure 7-2 on page 18 shows a photography of the complete application.

Figure 7-2. A Simple Application Using the Development Board for the ATA6602/ATA6603 (Photography)



8. Appendix

8.1 Schematic and Layout of the Development Board for the ATA6602/ATA6603

Figure 8-1. Schematic of the Development Board for the ATA6602/ATA6603

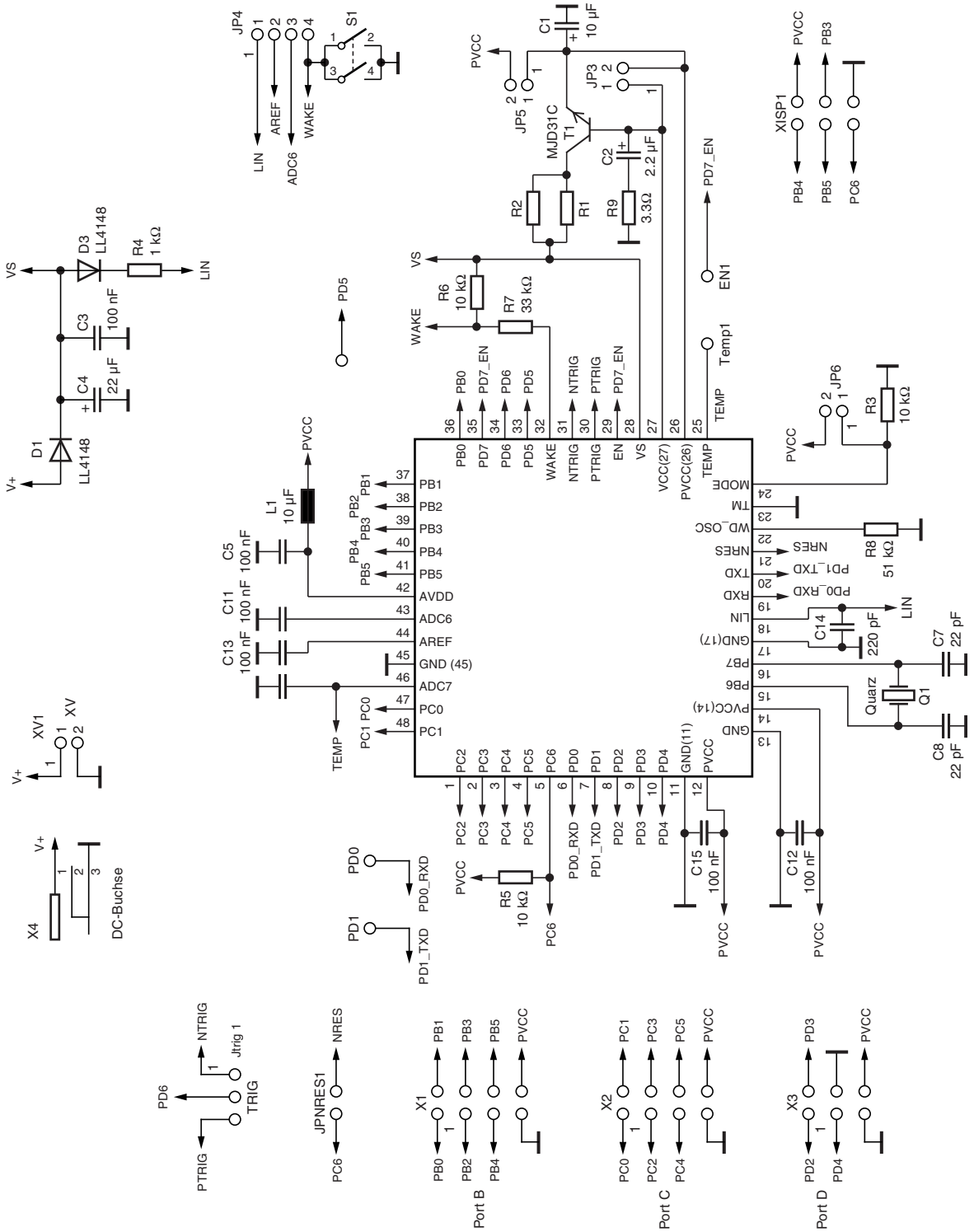


Figure 8-2. ATA6602/ATA6603 Board Component Placement; Top Side, Top View

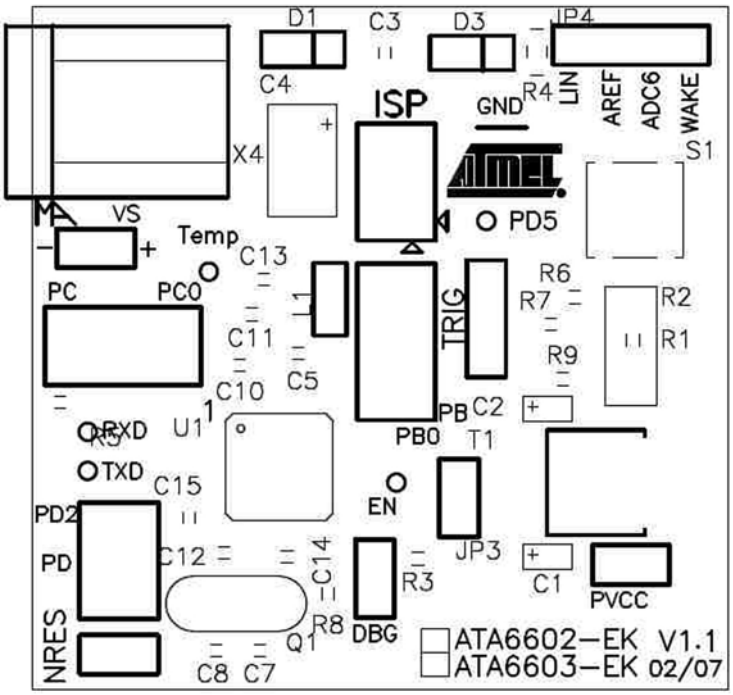


Figure 8-3. ATA6602/ATA6603 Development Board; Top Side, Top View

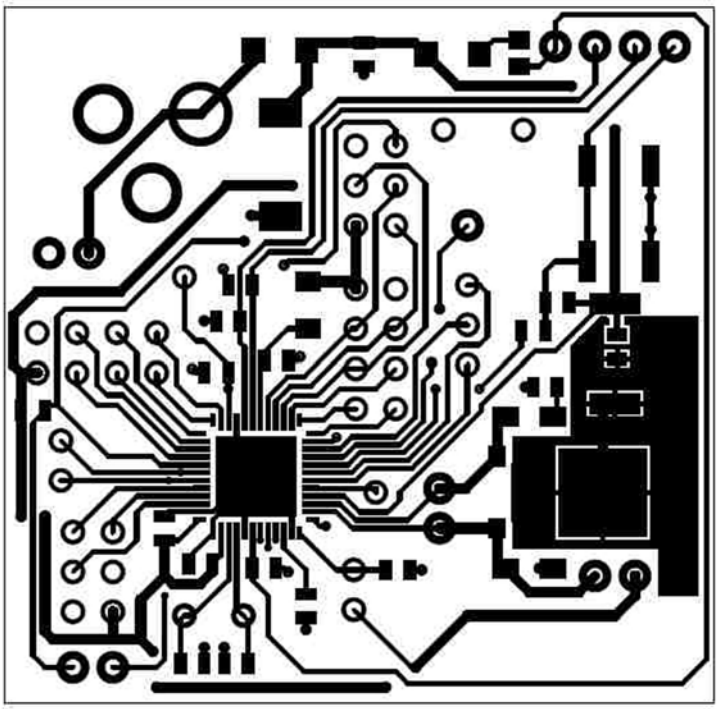
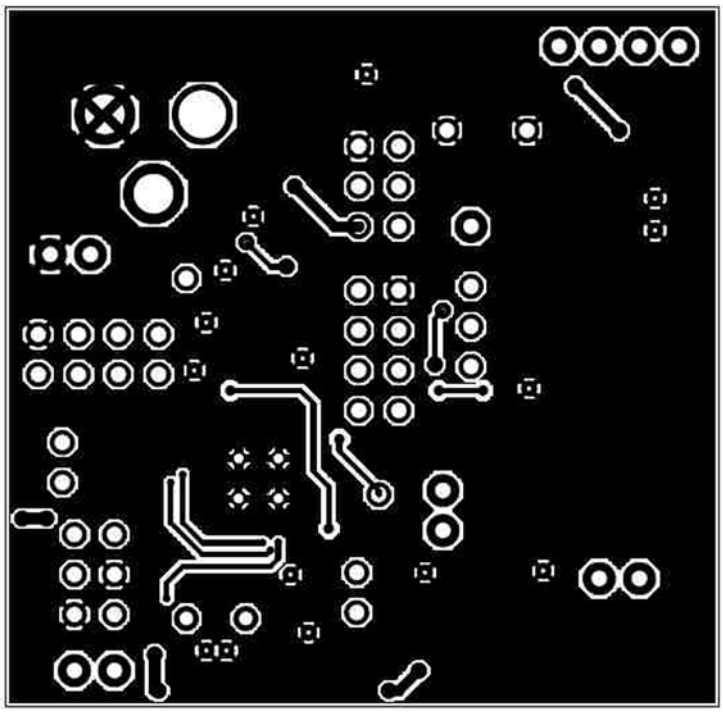


Figure 8-4. ATA6602/ATA6603 Development Board; Bottom Side, Top View



8.2 Additional Diagrams for the Internal Voltage Regulator

The diagrams below show the maximum output current I_{max} of the voltage regulator as a function of the supply voltage V_S at different coolings for thermal resistances R_{thJA} of the external NPN transistor T1.

Figure 8-5. I_{max} versus V_S at R_{thJA} = 80 K/W

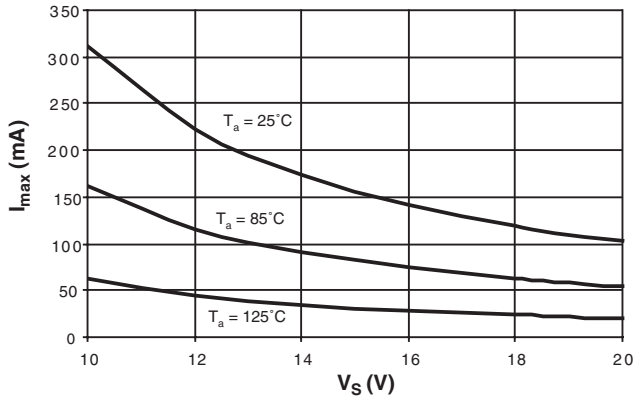


Figure 8-6. I_{max} versus V_S at R_{thJA} = 50 K/W

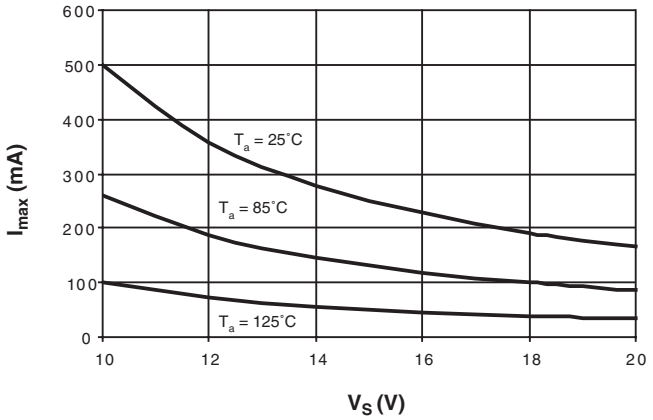
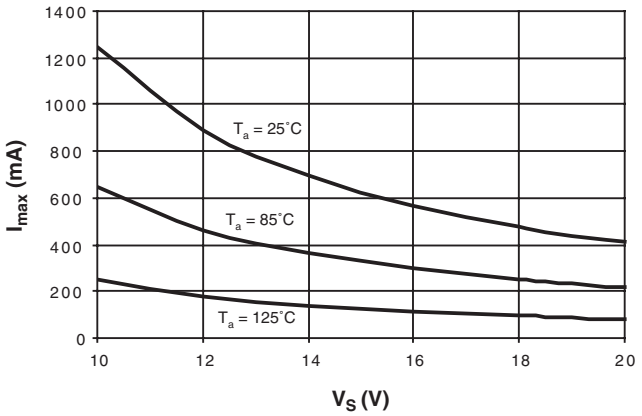


Figure 8-7. I_{max} versus V_S at R_{thJA} = 20 K/W



In the following diagrams some typical operating characteristics measured at the ATA6621 are shown. As the ATA6621 is included in both ATA6602 and ATA6603 without any change these measurements can be adapted without any restriction. The supply voltage VS is a diode forward voltage lower than VB (Reverse battery protection).

Figure 8-8. Output Voltage P_{VCC} versus Battery Voltage V_{bat} at Different Output Currents

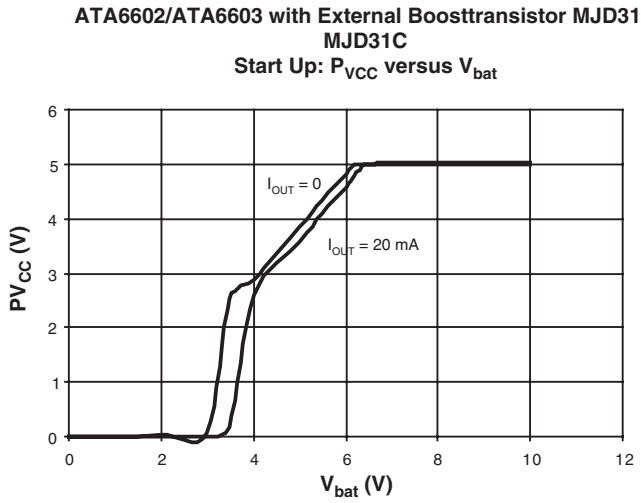


Figure 8-9. Output Voltage P_{VCC} versus Battery Voltage V_{bat} at Different Output Currents

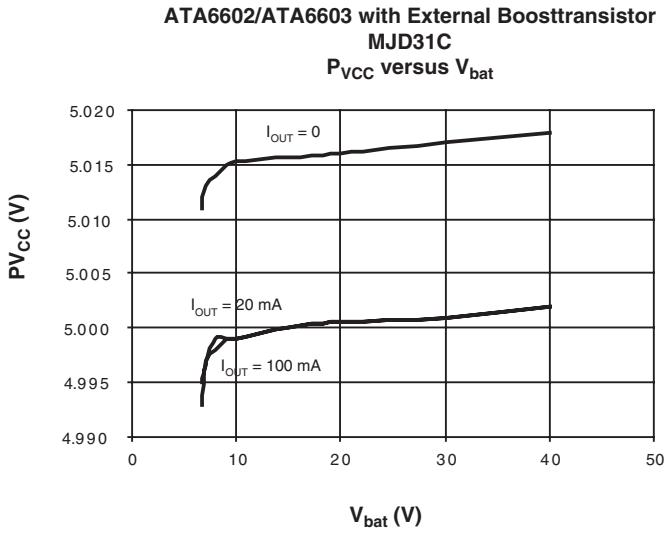


Figure 8-10. Load-transient Response with Channel 1 = I_{out} and with Channel 2 = P_{VCC}

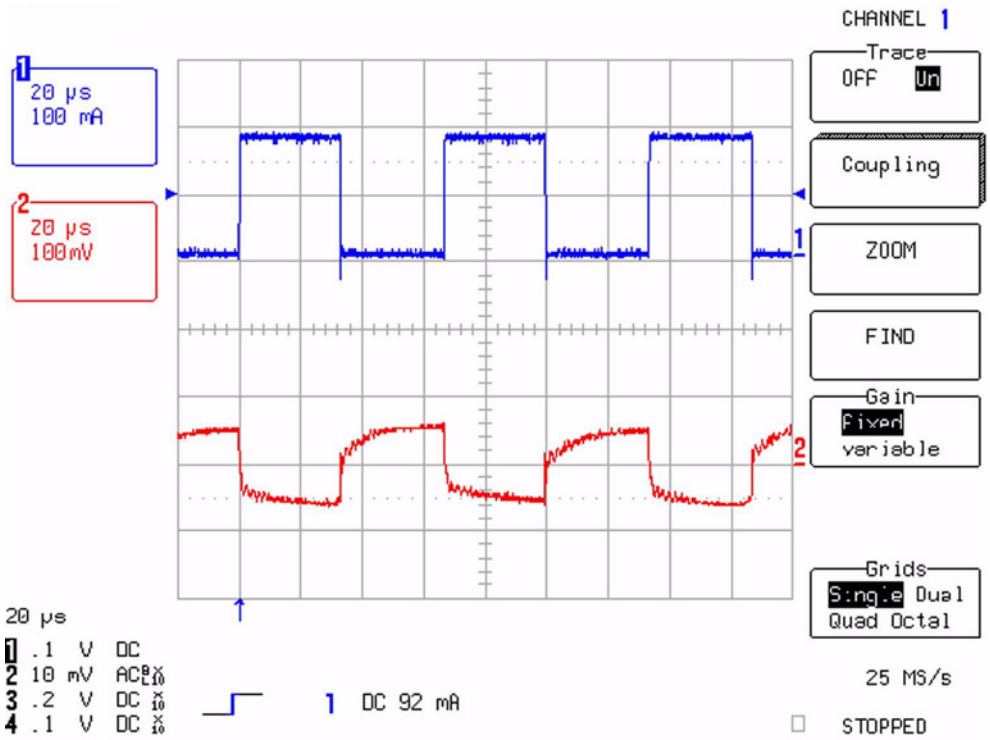


Figure 8-11. Start-up Response with Channel 1 = V_S and with Channel 2 = P_{VCC}

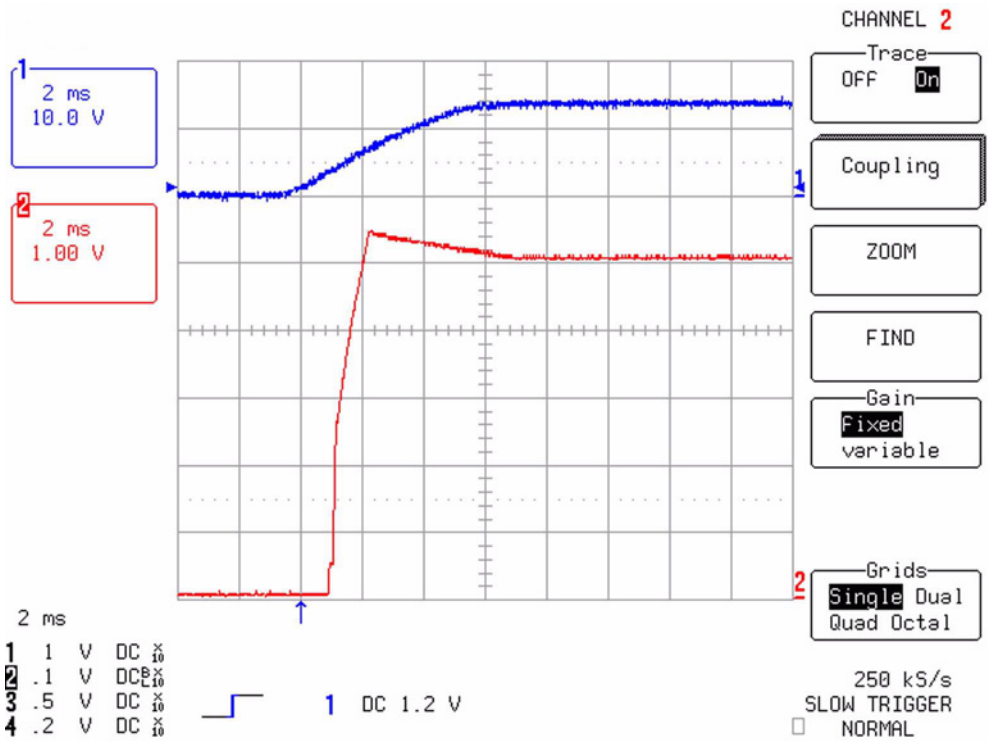


Figure 8-12. Switching from Silent Mode to Normal Mode with Channel 1 = NRES and with Channel 2 = P_{VCC}

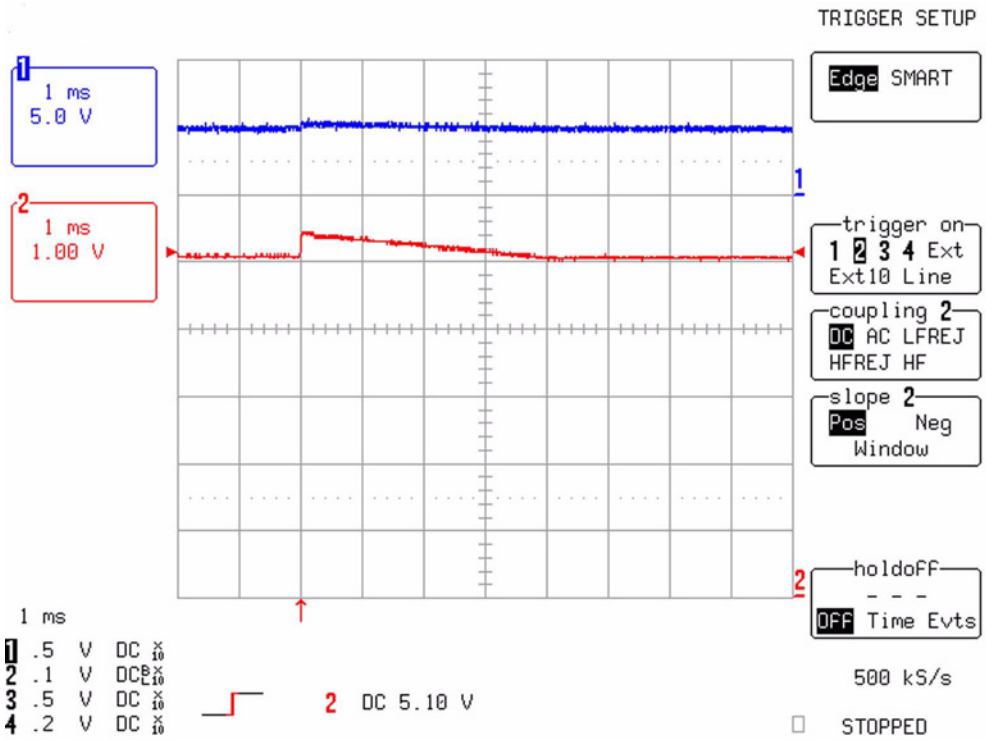
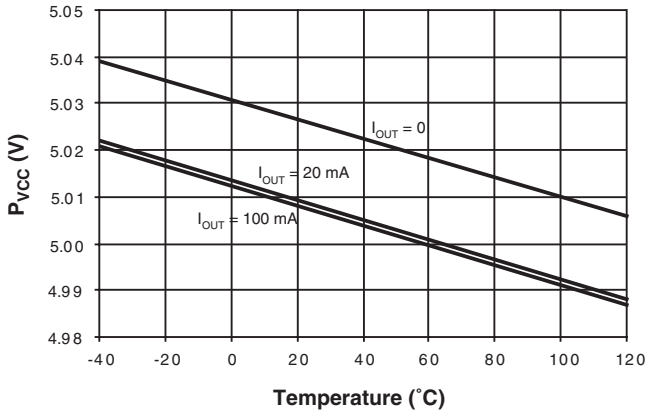


Figure 8-13. Output Voltage P_{VCC} versus Temperature at Different Current Loads



8.3 Further Information

8.3.1 Datasheets

1. http://www.atmel.com/dyn/resources/prod_documents/doc4921.pdf
   Datasheet ATA6602/ATA6603 complete version
2. http://www.atmel.com/dyn/resources/prod_documents/doc4887.pdf
   Datasheet ATA6621N complete version
3. http://www.atmel.com/dyn/resources/prod_documents/doc7530.pdf
   Datasheet ATmega48/88/168 Automotive
4. http://www.atmel.com/dyn/resources/prod_documents/doc7607.pdf
   ATmega88 Automotive - 150°C Specification - Appendix A Preliminary

8.3.2 Application Notes

1. http://www.atmel.com/dyn/resources/prod_documents/doc7653.pdf
   AVR140: ATmega48/88/168 family run-time calibration of the Internal RC oscillator

   This application note describes how to calibrate the internal RC oscillator via the UART. The method used is based on the calibration method used in the Local Interconnect Network (LIN) protocol – synchronizing a slave node to a master node at the beginning of every message frame.
2. http://www.atmel.com/dyn/resources/prod_documents/doc2554.pdf
   AVR095: Migrating between ATmega48, ATmega88 and ATmega168

   This application note describes issues to be aware of when migrating between the ATmega48, ATmega88, and ATmega168 microcontrollers.
3. http://www.atmel.com/dyn/resources/prod_documents/doc1637.pdf
   AVR308: Software LIN Slave

   This Application Note shows how to implement a LIN (Local Interconnect Network) slave task in an 8-bit RISC AVR microcontroller without the need for any external components.
4. http://www.atmel.com/dyn/resources/prod_documents/doc7548.pdf
   AVR322: LIN Protocol Implementation on Atmel AVR Microcontrollers

   The LIN protocol is introduced in this application note, along with its implementation on Atmel Automotive AVR microcontrollers.
5. http://www.atmel.com/dyn/resources/prod_documents/doc4938.pdf
   ATA6621 Truck Application

   This Application Note shows how to build up a LIN node for truck applications with the existing ATA6621 and therefore also with the ATA6602/ATA6603.

9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4999C-AUTO-03/08	• Section 1 “Introduction” on page 3 changed • Figure 3-3 “External Circuitry for a LIN Master Node” on page 12 changed • Section 4.2 “Debugging the ATA6602/ATA6603” on page 14 changed
4999B-AUTO-08/07	• Section 8.3 “Further Information” on page 26 changed

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